

IC 8D 16M 42 PIN ' 4 EPROM 32X R/D 837-11070 User's Manual Dos WR-9-02334

6 160 SHOU, AS ROOM Easter

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## 1.0 Overview

This is one of the circle used, in developing authorize for the Mega Drive/32X. Below is a list of its main destants.

Can mutall an EFROM of up to 64 Mb (8 MB) on the cond.
The EFROM used by this and uses the TCS7163010/TCS92000 series or
equivalent product. Access time uses a darker of 150 ns or less. This EFROM is
not attached.

2 An SRAM with a measurem of 256 KB and battery backup function is installed

 Using the bank select function, any EFROM can be selected and accessed in 4 Mart capts. Bank members are valid from 0 to 15 (When tased in 5 Mb(t) x 4 fermed, the bank mambers are valid from 0 to 7)

4 Power Supply: +SV DC is supplied from the main law.

5 Has a memory mode change function. Able to handle the conventional Mega Drives in Miles mode by changing awitches. The mode at factory dispenses in the 32 Meet mode.

Cax select the type of EPPCM table cited.
 Either 16 Mint- or 5 Mint-type EPRCM can be selected by charging DIP searches.

SC SD SSM 42 POX \* 4 EFROM SEX IND 837-10020 Day's Monad

### 2.0 Main Specifications Dowlant Morehers 830-11000 Printed Clarest Board Number 1714667 Memory Capacity. EPROM 64 M / 32 Mbs (processes area) SPAM 256 Khet (class great) Word Length 1 word 16 hits Memory Expandability Format Back Select I/O Specifications Conforms to Mess Drave pretended commo soccifications Card Diagnosions 96-5 (W) 150 (H) mm General logic pins TTL\_LSLECT TITROM TC57162000-150 / TC5796000-150 SRAM 10MO056 CLEP 13. (Hough) controlled medical Custom IC. 255-8709 (See a) Battery CR2002 (Nory) equipment per saftery nor ked EEP made by our Power supply:

APL SH or less



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#### 3.0 Description of Functions

This ROM could in partitioned and managed in 4 Met memory siderases (Senk 0 bink 11, 64 Mello). The Mega Derre curtifiege rate is partitioned into cight accus, each having 6 Metes. Only ered 6 with vector in funds, any book can be allocated to the minimizing seriou awas. Basics are specified by the brack sorting regulators (AUSCHI - AUSWIFF) and addressings of the Mega Defree).

Bit 0 of register 0 is the address following 200000H used in switching the ECBM/ backup RAM. Bit 1 of register 0 is used in setting the backup RAM write protect Recease there is no birsk for the backup RAM, addresses after 200000H become straight backup RAM area.

Such mambers writing in nighter 1 through regaler 7 correspond to their respective areas area 1 through rest 7 these members can be set from 0 to 63, however, with this 82M cord, only the FPRCM-restabled basis reserves are wish.

When few is Mer JFROMs are used and of Motar are feature, beak surface from the 13 are effective and the new soll or infantive properly, for any other setting. When few 5 More IFFROMs are used and 22 Mele are leaded, beak members from 5 or 7 are effective and the roar with an Interactive property from order setting. When the property is break or executive to consider some 3 order setting. When the property is break or a result, the consideration processes 23 Mele SOM model (see 1 - sent). The LT 1 - leak A 7 years and which present rise for lawking EAMs is standed of The Annual Consideration of the Consideratio

The next page shows the relationship of the MD cartridge sees and bank setting require:





Status when the power is turned on or reset.



IC SD HM @ RN 14 FPROM DY KIN

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# 3.1 Using the 16 Mbit ROM Mode + Backup RAM

The Configuration of the Confi

This applies to 0000001 - IPPTFTH SOM area and 200000H to bedoup RAM area. That type of memory allocations in called the 1600 mode. Improper operation occurs if a basis register is therefore in this mode.





Two DIF switches are designed on the card and for 32 Mbst or 16 Mbst memory mode. The factory setting is 32 Mt mode for 16 Mbsthave \$250 CM ray 6 M Mode (User settings) Use 16 Mbst-trae EPROM 22 M Mode /Clear summer e-track EPROM AC NO THAN 40 PRIC\* 4 EPIKONI KIN BAD

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2.3 Description of Each Switch Two DIP exercises, SW(4) and SW(38, are designed on the circle. The function of dance awatches are explained below. SW141 (Memory mode setting switch)

. Switches 1 to 3 Used in the chip select signal switch of SRAM/ETROM • Switch 4 Not in use. Normally turned OFE. • Switch 5

Select whether to allow/disallow operation of the bank ougster

CN Bank register operation allowed. CFF Bank register operation not allowed. Serral connection change with consideration to return devices

•Switch 6 CIFF -CART signal not converted. STATUS (EPROM type setting switch)

· Switches 1 to 4 Used in the 35 Mbit type STROM chip white a Correspond respectively to IC1 through IC6 Swetchen 5 to 8 Used in the 8 Mbst type SPROM divinations alread water-

### 4 n EPROM Mounting

This EPROM card includes K' sockets K' 1 through K' 4 Programmed EPROMs or inserted in IC sockets and used. Because EPECMs used on this EPR Mbst/8 Mbst (2 Mbyse/1 Mbyse), a monumen of one chap should be more ROM banks and their corresponding chaps are shown below

## 6 Mbs: type (TC5782000)

ICI mount (Uttas) Accommodates bank 0 and hunk 1 IC2 mount (UCG) Accommodates bank 2 and bank 2 903 mount (13027)

#### IC4 mount (U028) \* 16 Met two (ECS71653011)

IC1 mount (U025) K2 moure (Ut26)

IC4 mount (T128)

ank 8 to bank 11 sk 12 to bunk 15 The illustration on the next pure shows the incursor of EFR

Note: Selve murphing on \$19000, make sum to check

5.0 Yeav (Front View) SEGA 171-6967



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